Presenter:
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Behavioral models of power RF GaN Transistors

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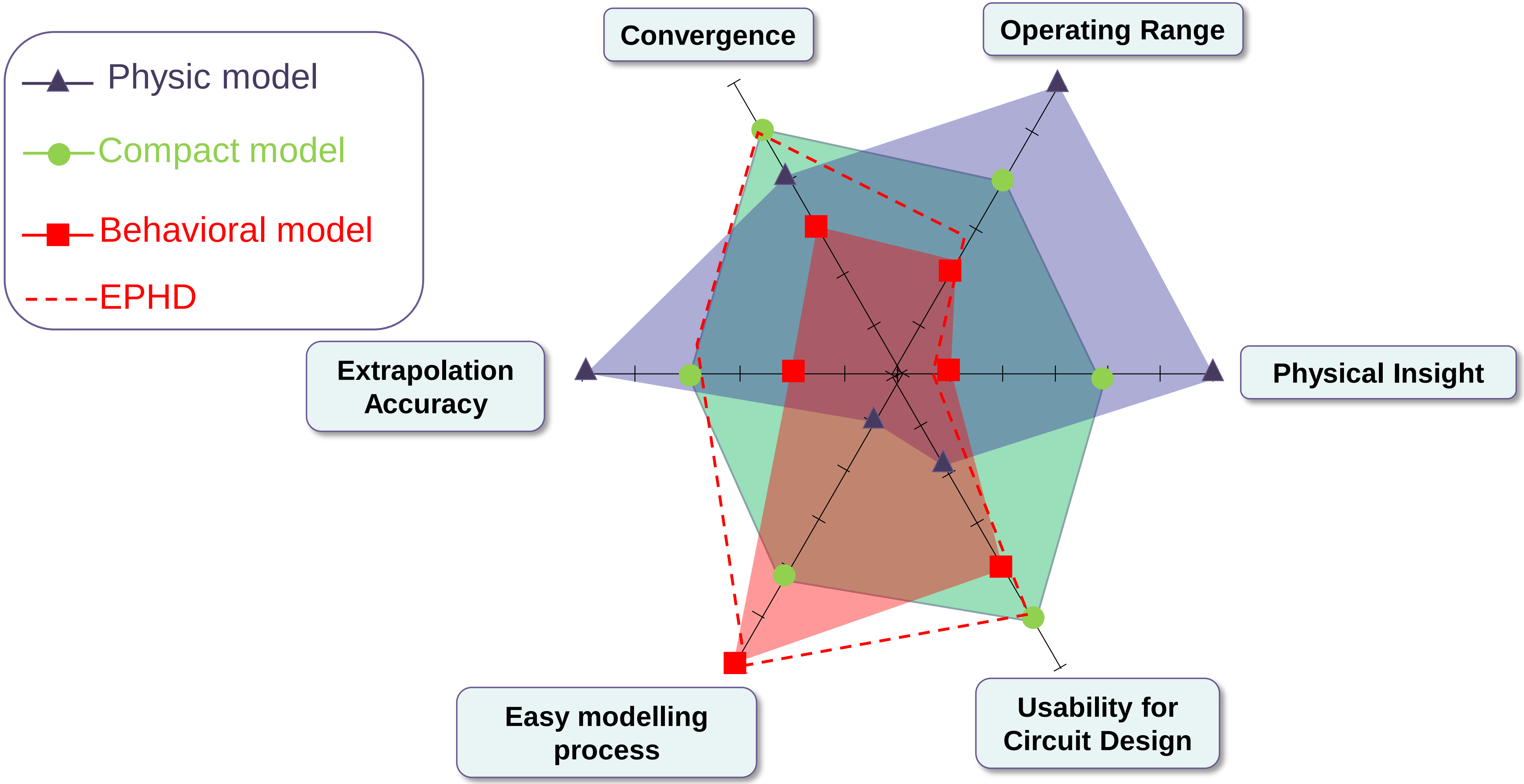
Agenda

- EPHD description
  - Types of larges Signal transistors model
  - Motivation
  - Theory
- EPHD model packaged transistors example
- Benchmarking X-parameter vs EPHD
- Measurement bench & Methodology

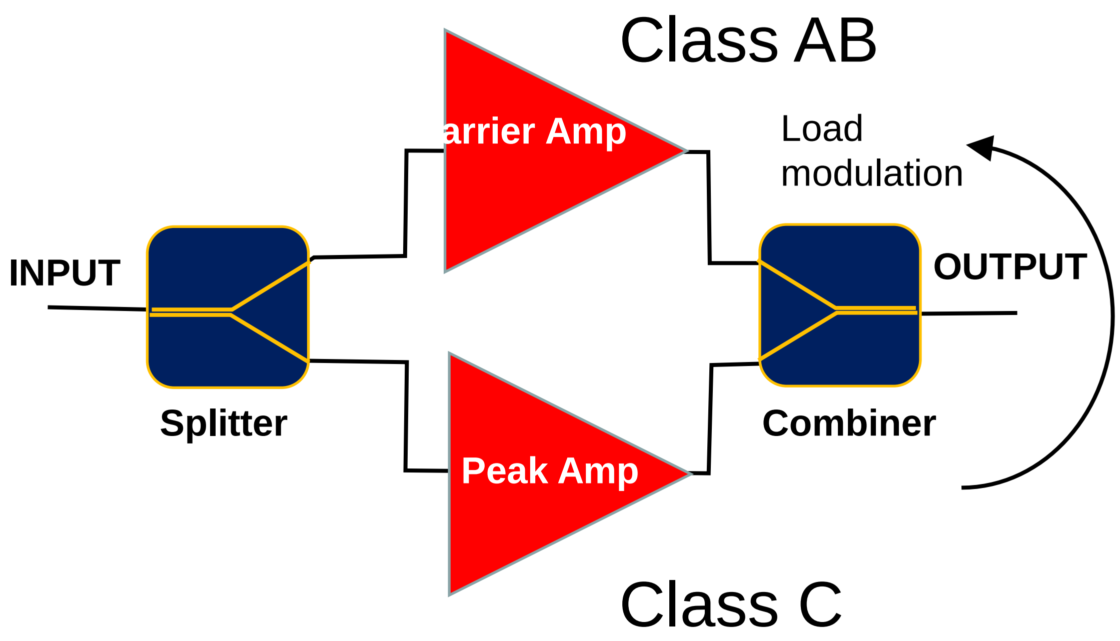
- EPHD description
- EPHD model packaged transistors
- Benchmarking
- Measurement Bench & Methodology

Types of Large-Signal Transistor Models



Motivation

Hybrid Doherty Amplifier Design using a packaged device



Load Pull measurement only ?

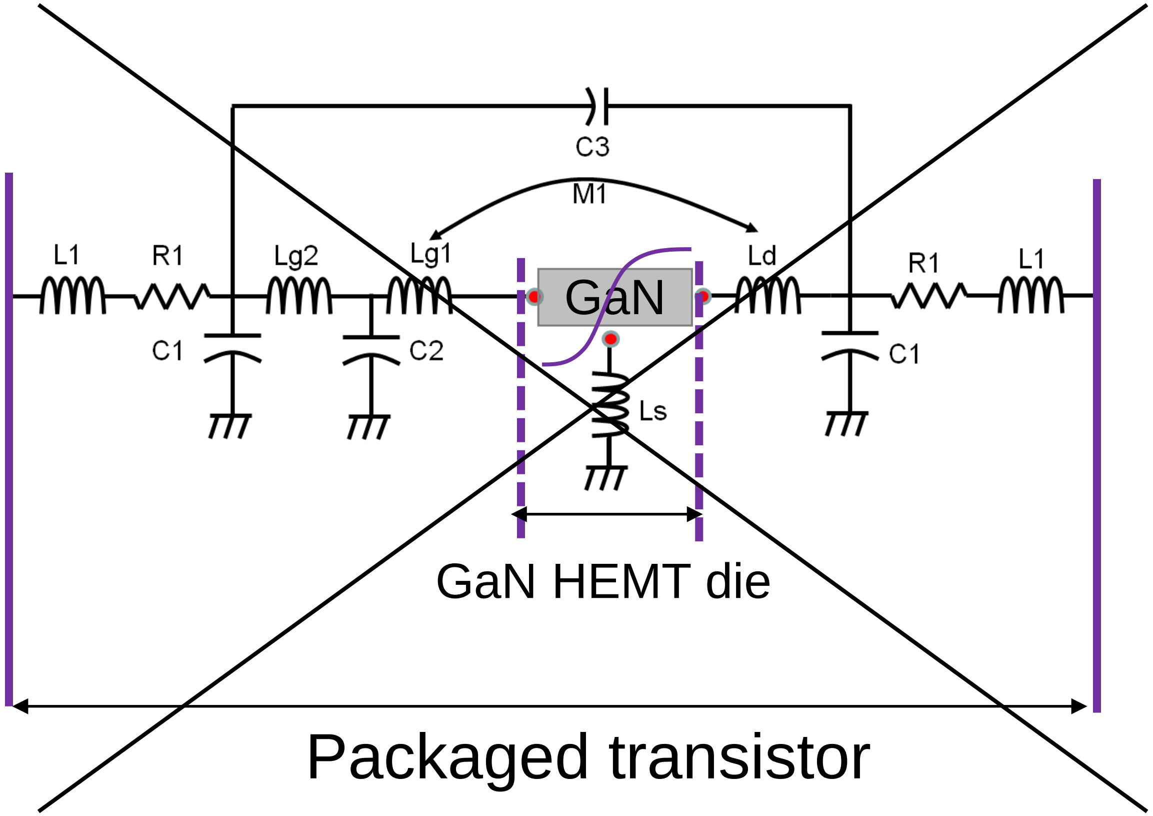
- No : Load Modulation

Transistor model requirement:

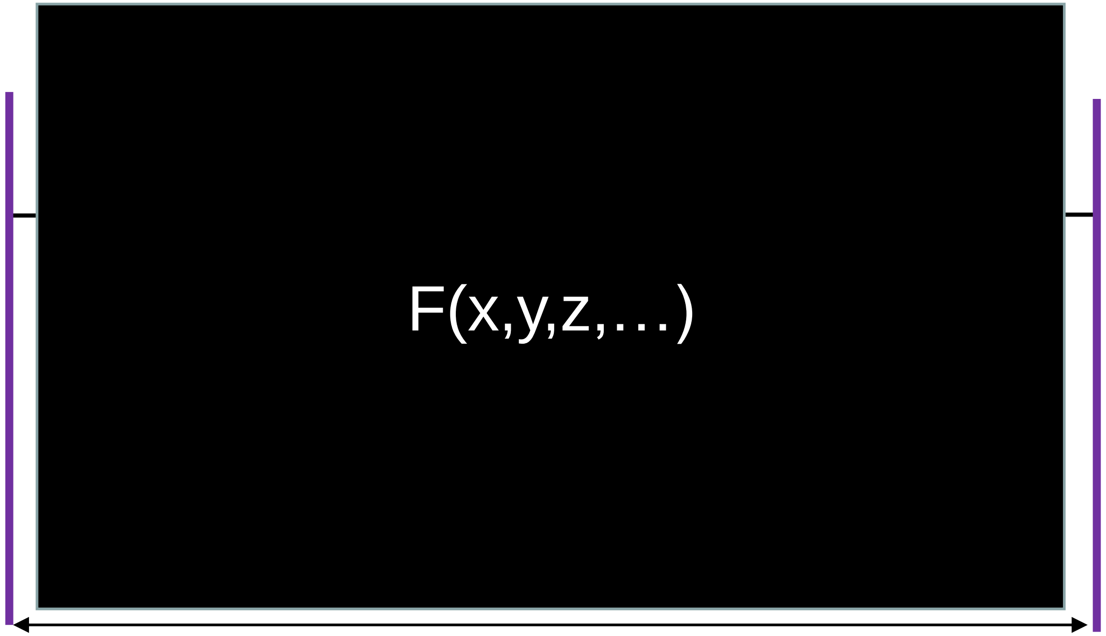
- Accuracy over a wide dynamic range
- Accuracy over different load conditions
- For different class of operating conditions

Compact Model

Black Box Model



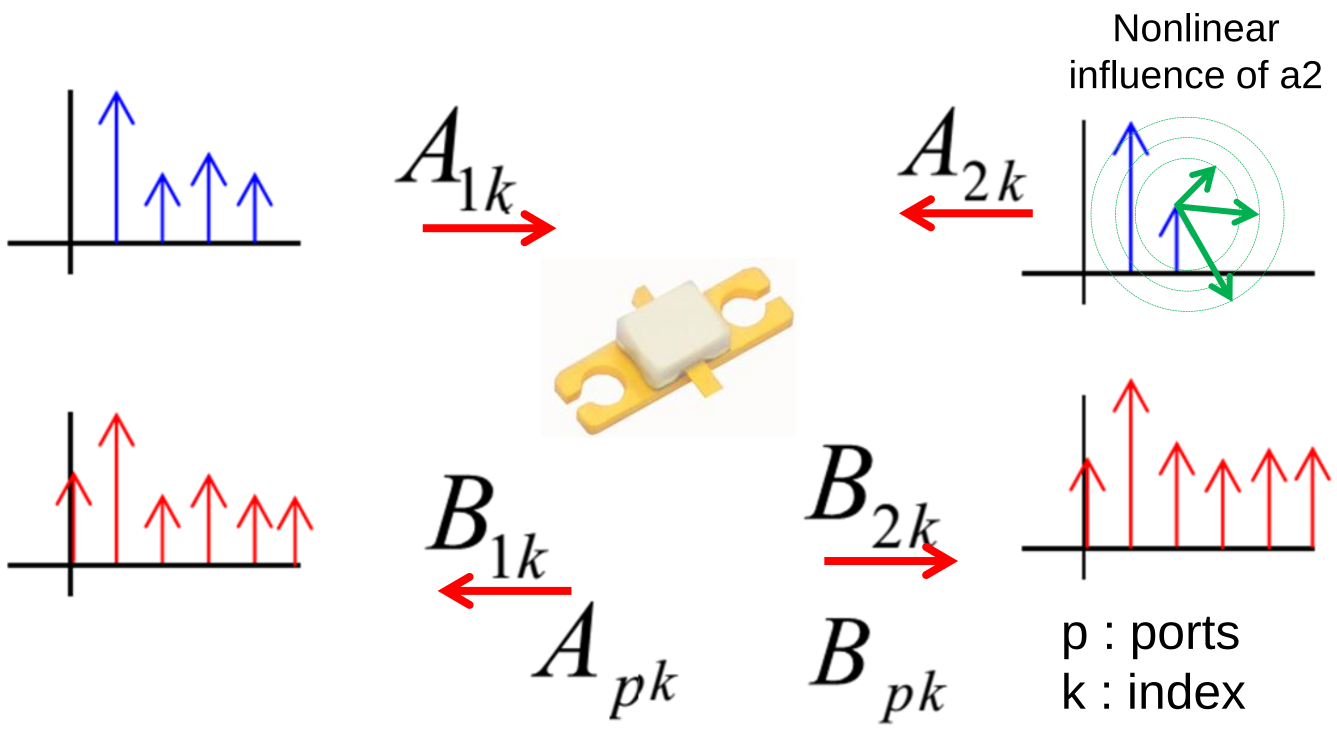
All package elements are finally fitted by comparison between measured and simulation



Packaged transistor

Set of equations

Enhanced Polyharmonic Distorsion model



Harmonic superposition
3rd order expansion !

- The model is extended to the third order
- Bi(t) is the ∑ of f0 and harmonic modulated tones
- The main nonlinearities are driven by the incident power wave @f0 at the input port

$$\widetilde{b_{ik}(t)} = S_{ik,11,1}\left(\left|\widetilde{a_{11}(t)}\right|\right)\widetilde{a_{11}(t)} + S_{ik,21,1}\left(\left|\widetilde{a_{11}(t)}\right|\right)\widetilde{a_{21}(t)} + T_{ik,21,1}\left(\left|\widetilde{a_{11}(t)}\right|\right)p^{k+1}\widetilde{a_{21}(t)}^{*}$$

Order 1

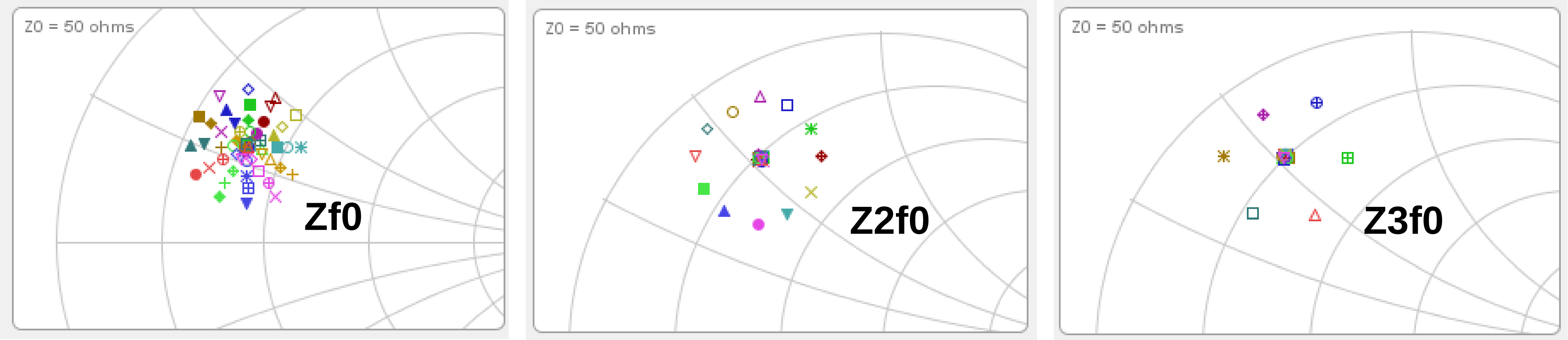
$$+ S_{ik,21,2}\left(\left|\widetilde{a_{11}(t)}\right|\right)p^{-1}\widetilde{a_{21}(t)}^{2} + T_{ik,21,2}\left(\left|\widetilde{a_{11}(t)}\right|\right)P\,\widetilde{a_{21}(t)}\,\widetilde{a_{21}{}^{*}(t)} + U_{ik,21,2}\left(\left|\widetilde{a_{11}(t)}\right|\right)p^{3}\widetilde{a^{21^{*}}(t)}^{2}$$

Order 2

$$+ S_{ik,21,3}\left(\left|\widetilde{a_{11}(t)}\right|\right)p^{-2}\widetilde{a_{21}(t)}^{3} + T_{ik,21,3}\left(\left|\widetilde{a_{11}(t)}\right|\right)\widetilde{a_{21}(t)}^{2}\,\widetilde{a_{21}{}^{*}(t)} + U_{ik,21,3}\left(\left|\widetilde{a_{11}(t)}\right|\right)p^{2}\widetilde{a_{21}{}^{*}(t)}\,\widetilde{a^{21^{*}}(t)}^{2} + W_{ik,21,3}\left(\left|\widetilde{a_{11}(t)}\right|\right)p^{4}\widetilde{a_{21}(t)}^{3}$$

Order 3

Measurement Process for model extraction



For each fundamental frequency, a pattern of load impedances is proposed, as follow :

- [**49** $Zload_{f0}$] & [$Zload_{2f0} = Z_{ref}$] & [$Zload_{3f0} = Z_{ref}$]
- [$Zload_{f0} = Z_{ref}$] & [**7** $Zload_{2f0}$] & [$Zload_{3f0} = Z_{ref}$]
- [$Zload_{f0} = Z_{ref}$] & [$Zload_{2f0} = Z_{ref}$] & [**7** $Zload_{3f0}$]

Behavioural models of power RF GaN Transistors

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EPHD

- Higher order of nonlinearity

PHD

Measurement extraction speed

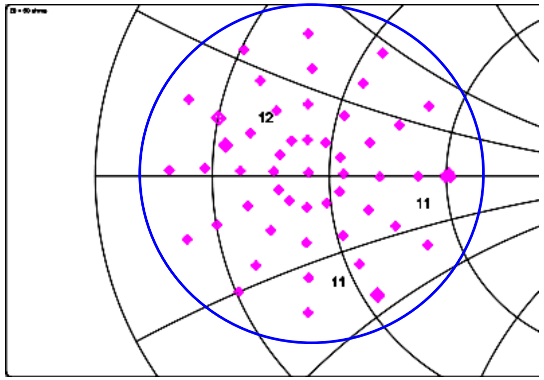
Measurement can be time consuming

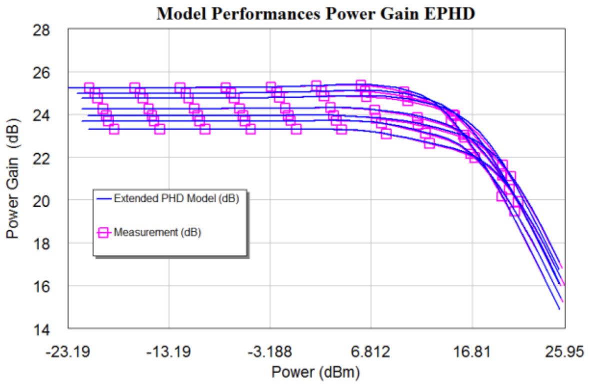
Model Validity

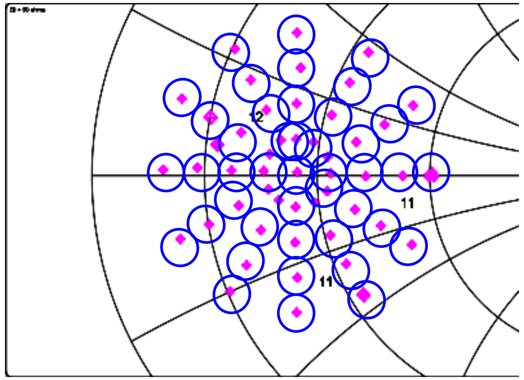
○ Area of Model Validity

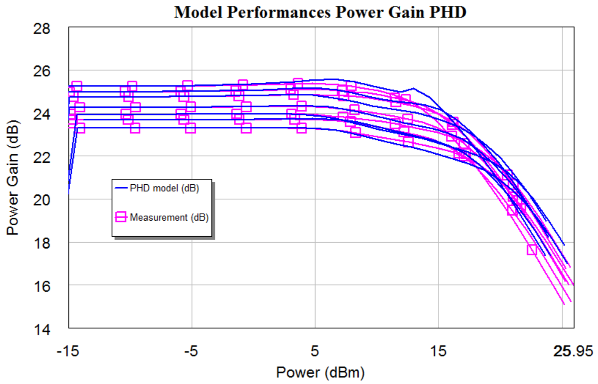
- More robust for interpolation and extrapolation

- Interpolation linked to the density of the grid
- Juxtaposition of several models









EPHD description

Benchmarking

EPHD model packaged transistors

Measurement Bench & Methodology

Impedance configuration

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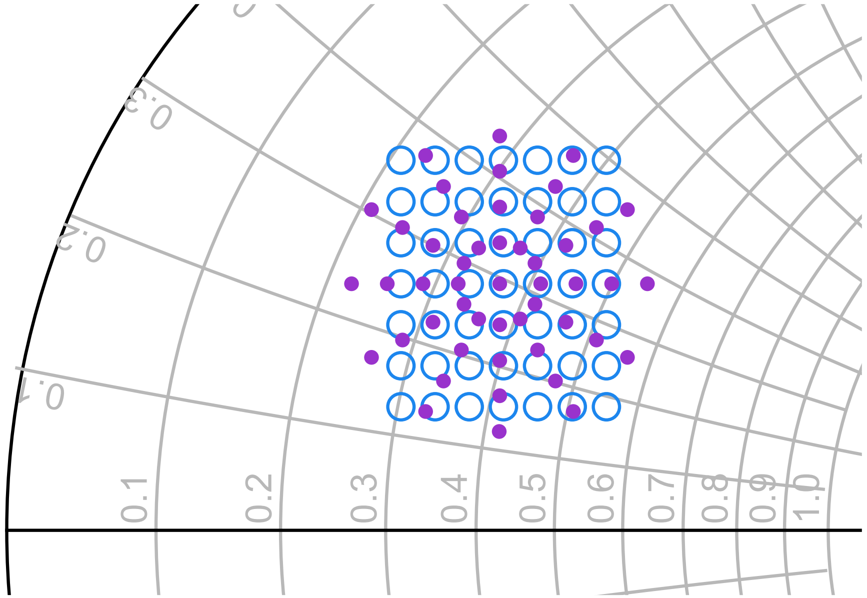
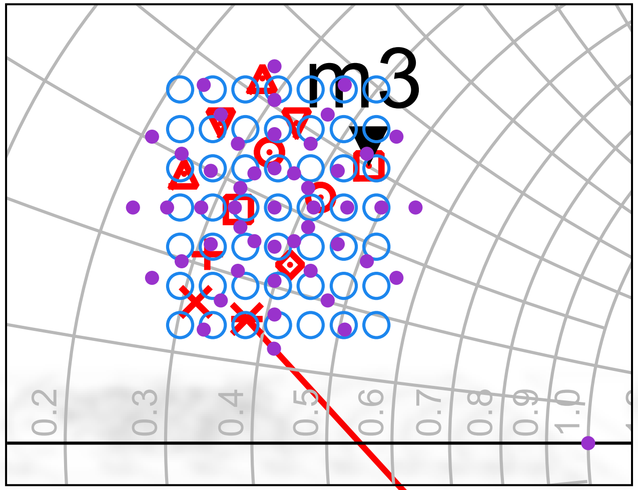
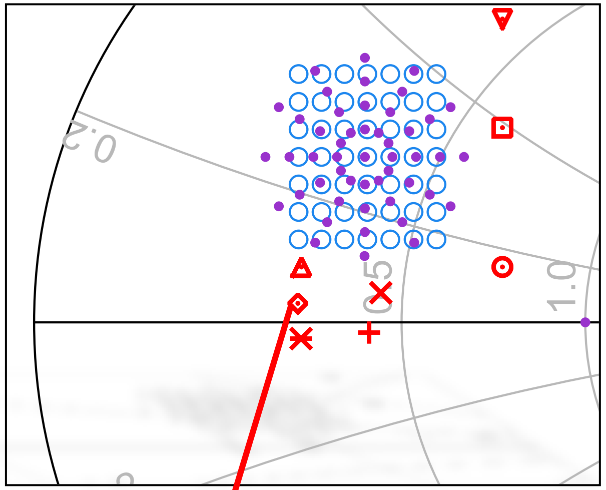
- Reference : Compact Model CREE CGH40
- Model extraction with similar points density(≈ 49 impedances @ f0)
- Same load impedances @2f0 & 3f0



Interpolation capabilities



Extrapolation capabilities



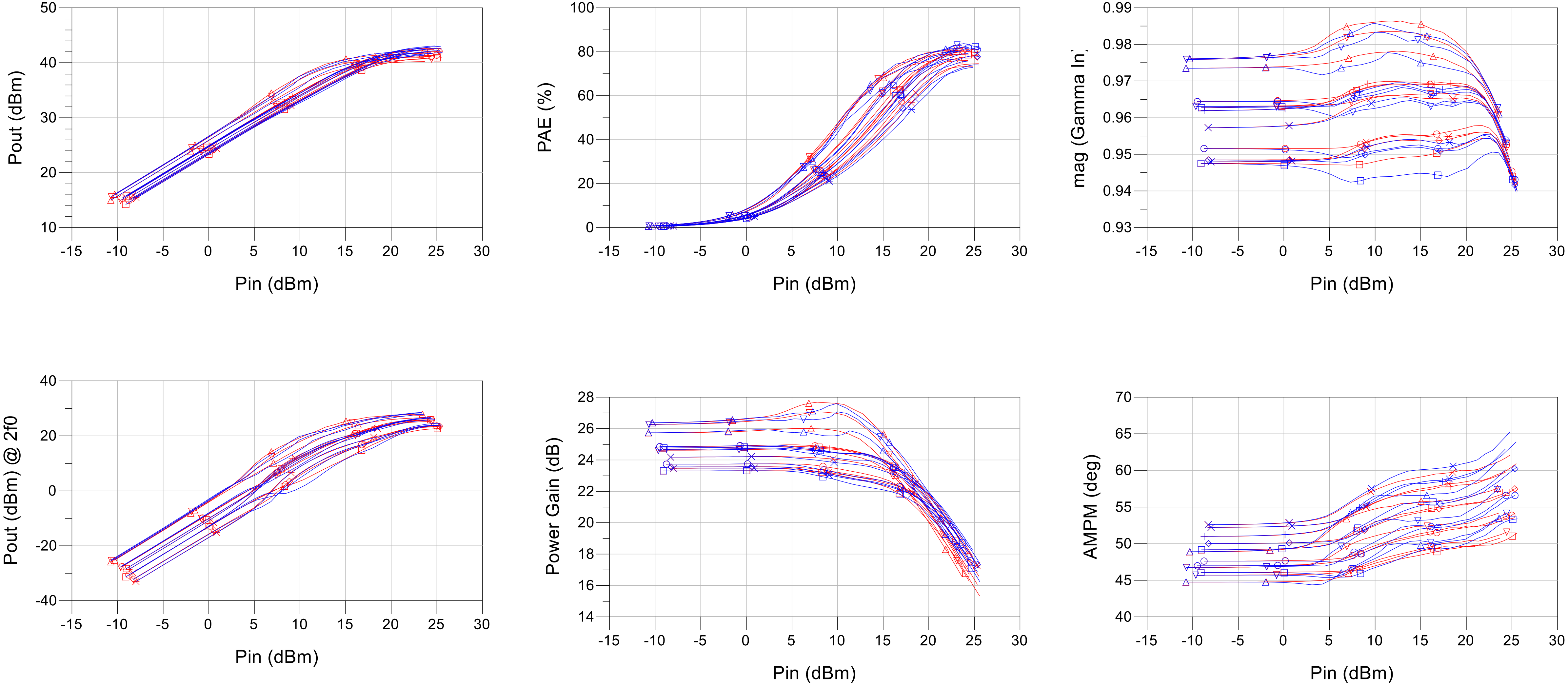
Tests conditions

X-parameters extraction area

EPHD extraction area

Class AB model : X-parameters

Interpolation



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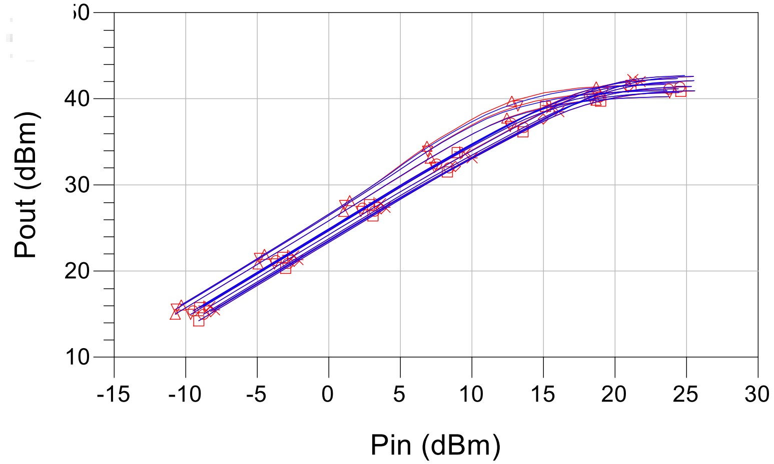
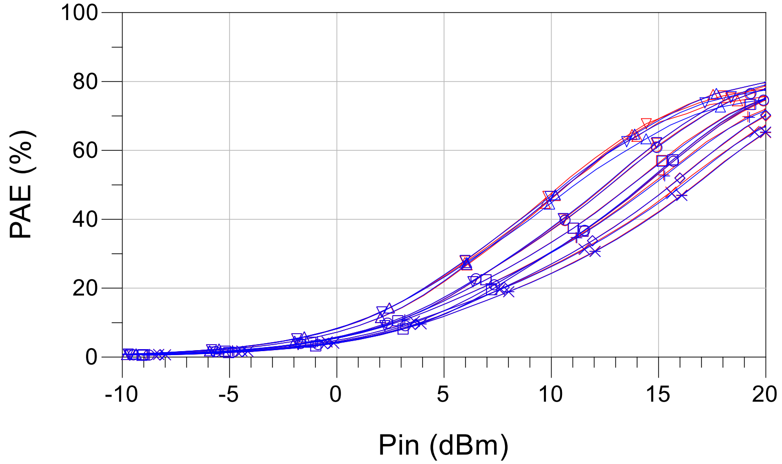
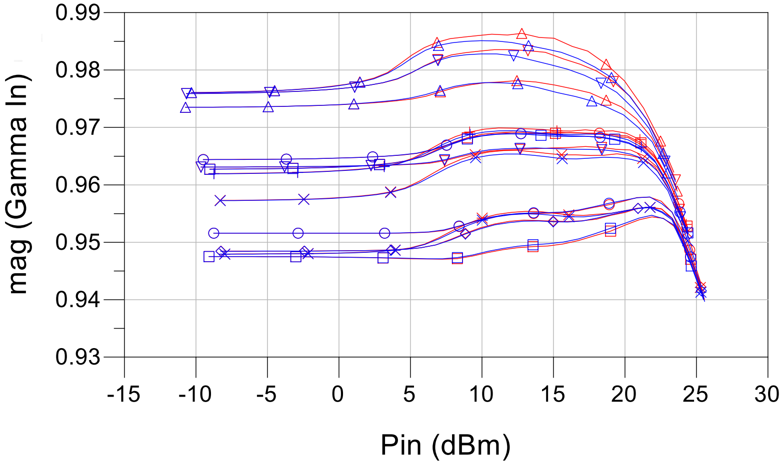
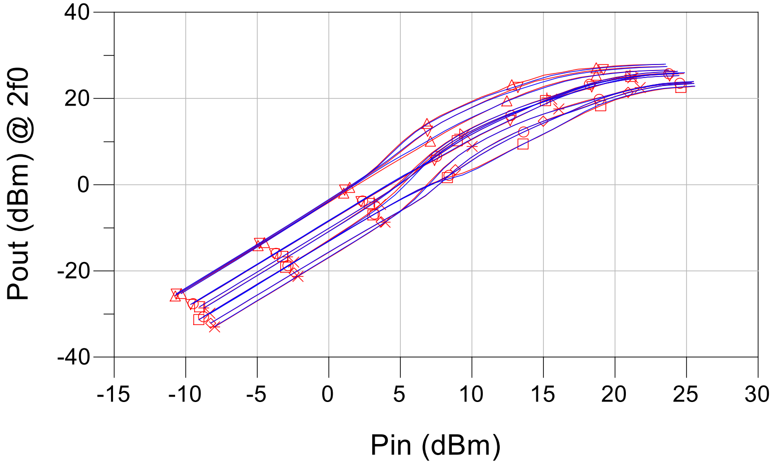
Class AB model : EPHD

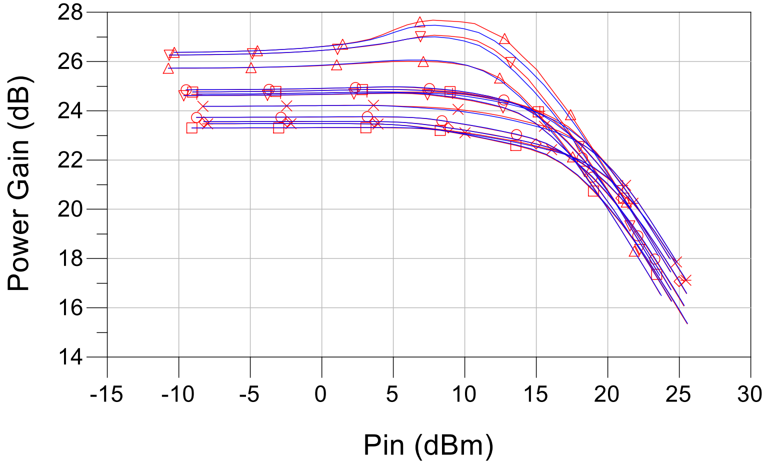
Interpolation

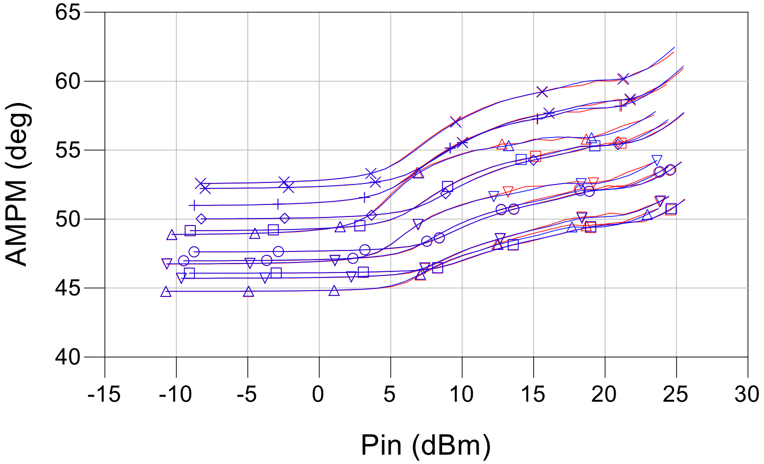












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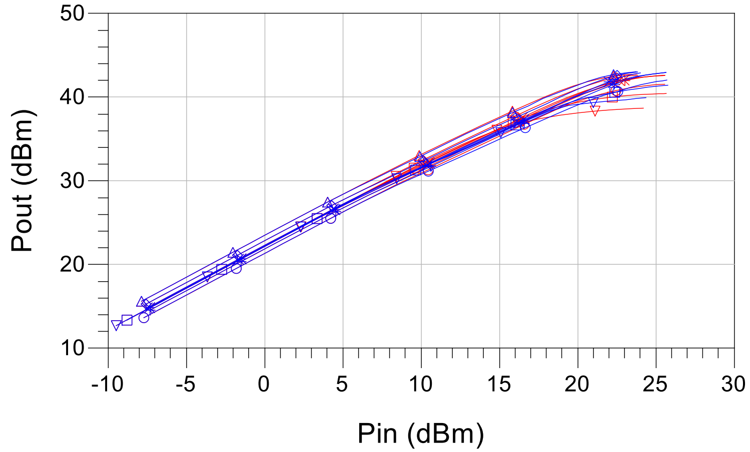
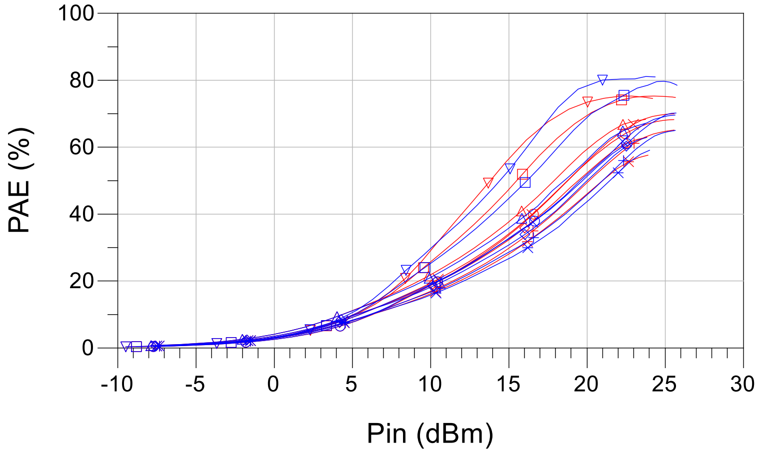
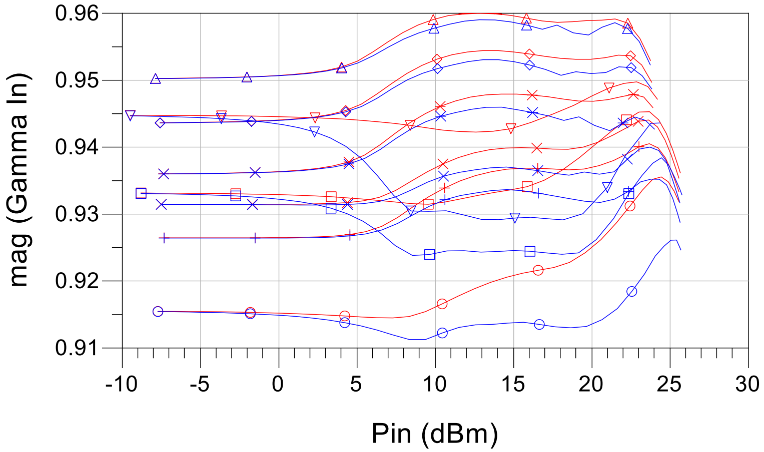
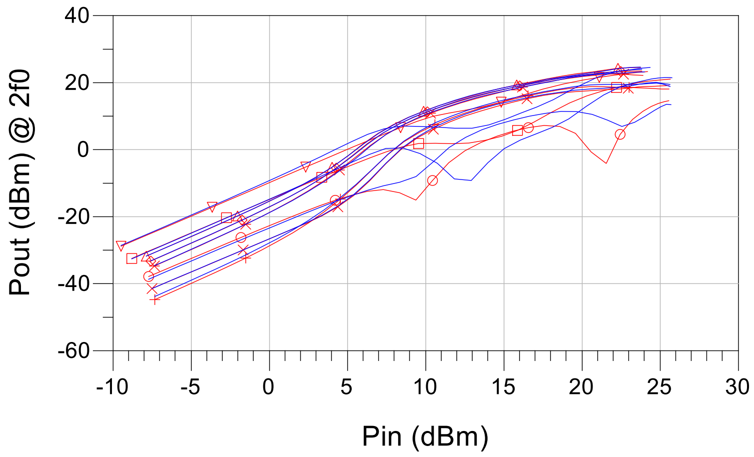
Class AB model : X-parameters

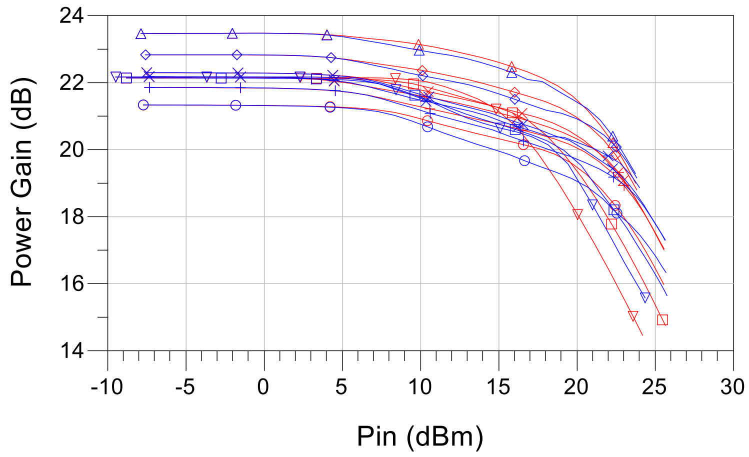
Extrapolation

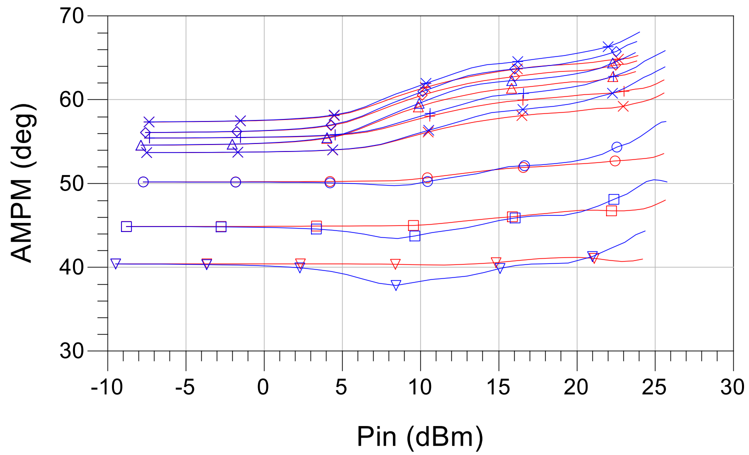






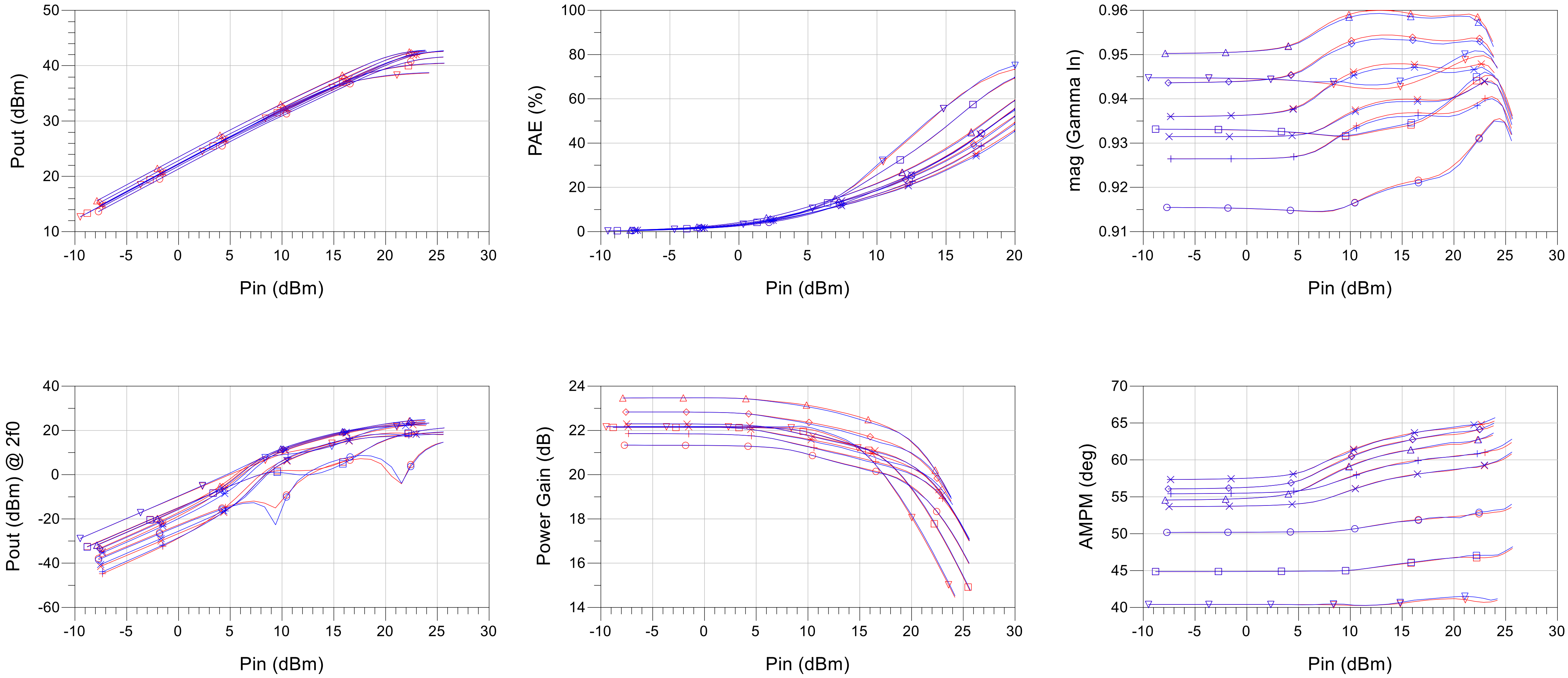






Class AB model : EPHD

Extrapolation



Benchmarking Conclusion

- EPHD ensure more accurate interpolations in areas where the gain & current curvatures have sharp variations
- EPHD predictions are more accurate in load extrapolation conditions due to the higher order of nonlinearity description.
- For low input impedance areas, or negative input impedances, X-parameters formalism does not allow to run a proper model extraction
- Both models allow good simulation convergence
- Extraction time for X-parameters is higher than the extraction time for EPHD (measurements)
- Accurate to simulate harmonic behavior

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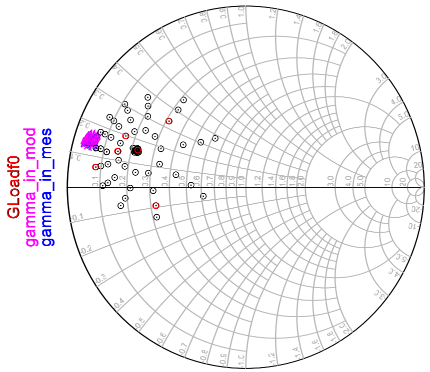
- EPHD description
- Benchmarking
- **EPHD model packaged transistors**
- Measurement Bench & Methodology

EPHD: Model vs Measurement

- **Class AB model @ 3,7GHz**

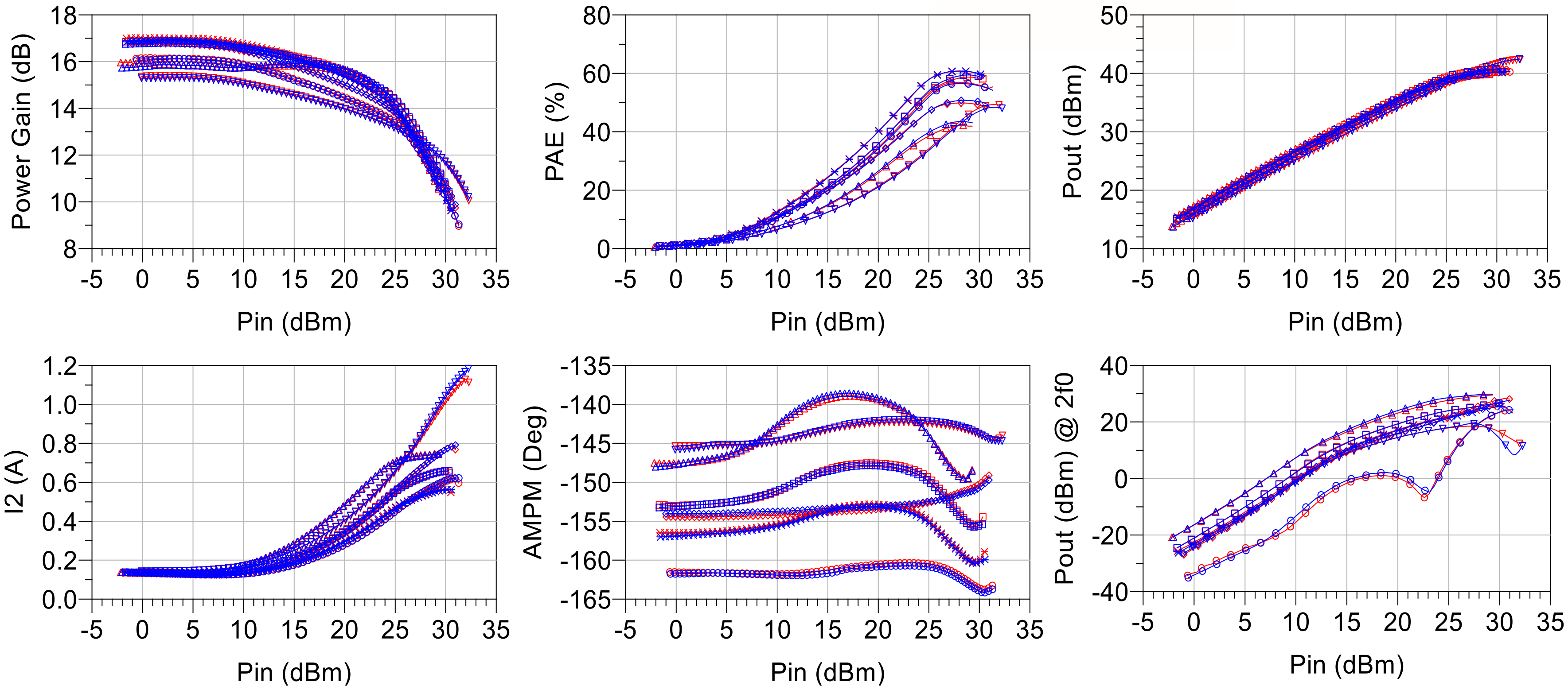
EPHD

Measurement



The model is able to reproduce the measurements which have been used for the model extraction

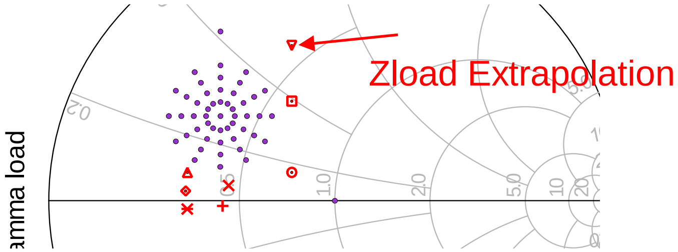
Class AB



EPHD: Model vs Measurement

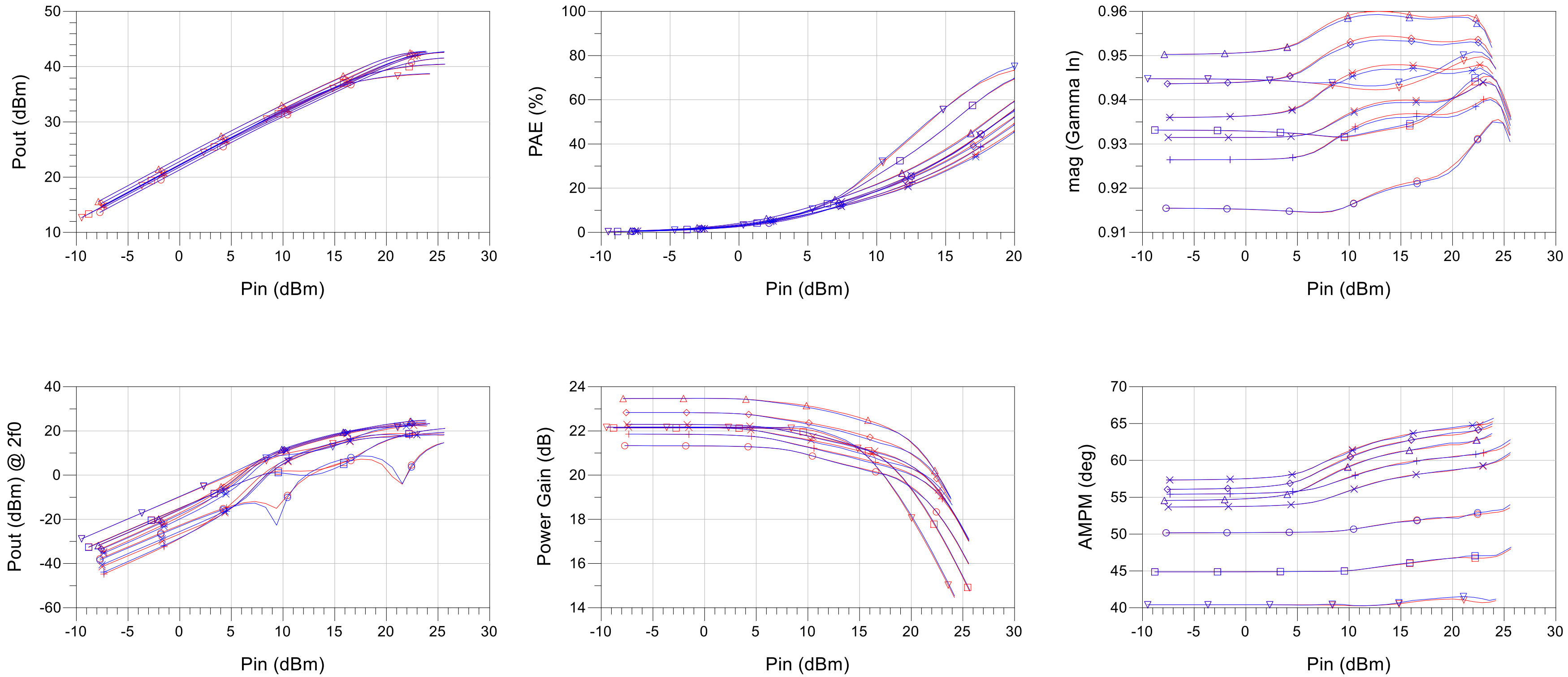
- **Class AB model @ 3,7GHz**

EPHD
Measurement



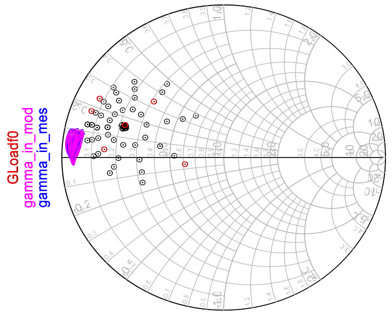
The model is able to reproduce the measurements which have **NOT** been used for the model extraction

Class AB



EPHD: Model vs Measurement

- **Class C model @ 3,7GHz**



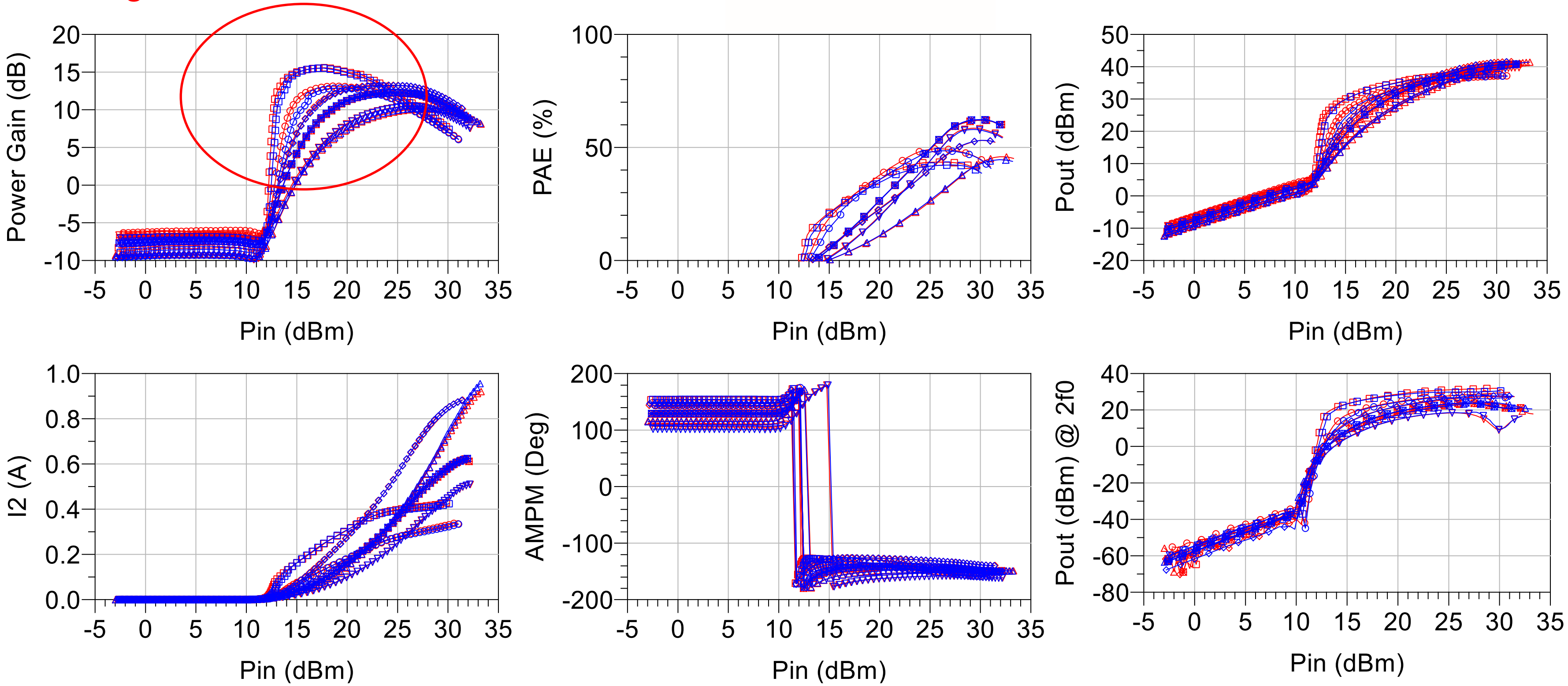
The model is able to reproduce the measurements which have been used for the model extraction

Class C -> see Power Gain curve shape

EPHD

Measurement

Strong nonlinear behavior

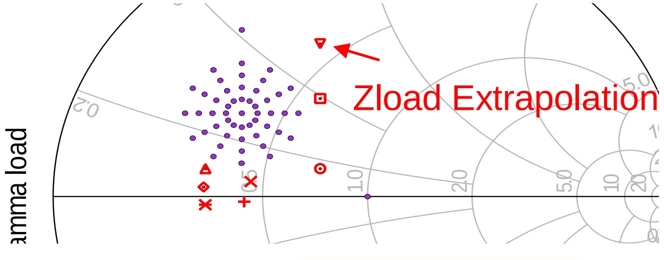


EPHD: Model vs Measurement

- **Class C model @ 3,7GHz**

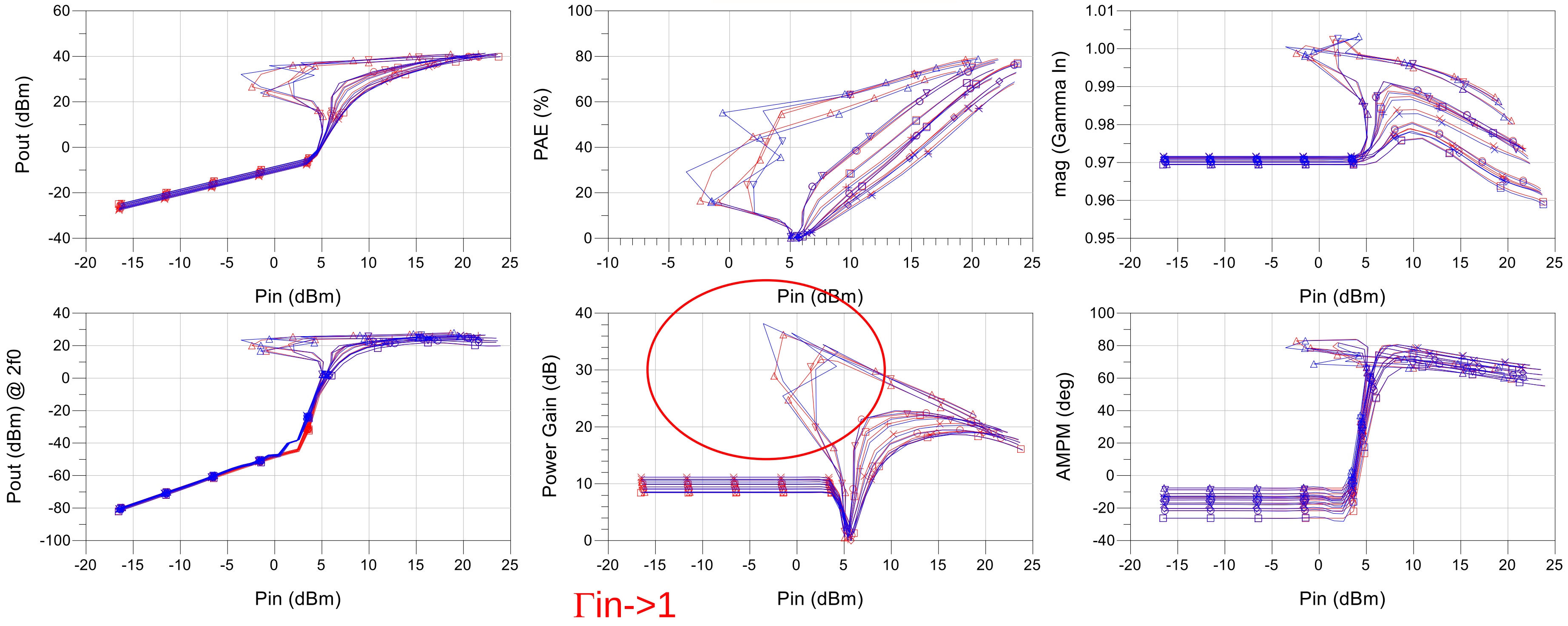
EPHD

Measurement



The model is able to reproduce the measurements which have NOT been used for the model extraction

Class C -> see Power Gain curve shape



EPHD: Frequency Interpolation Capabilities

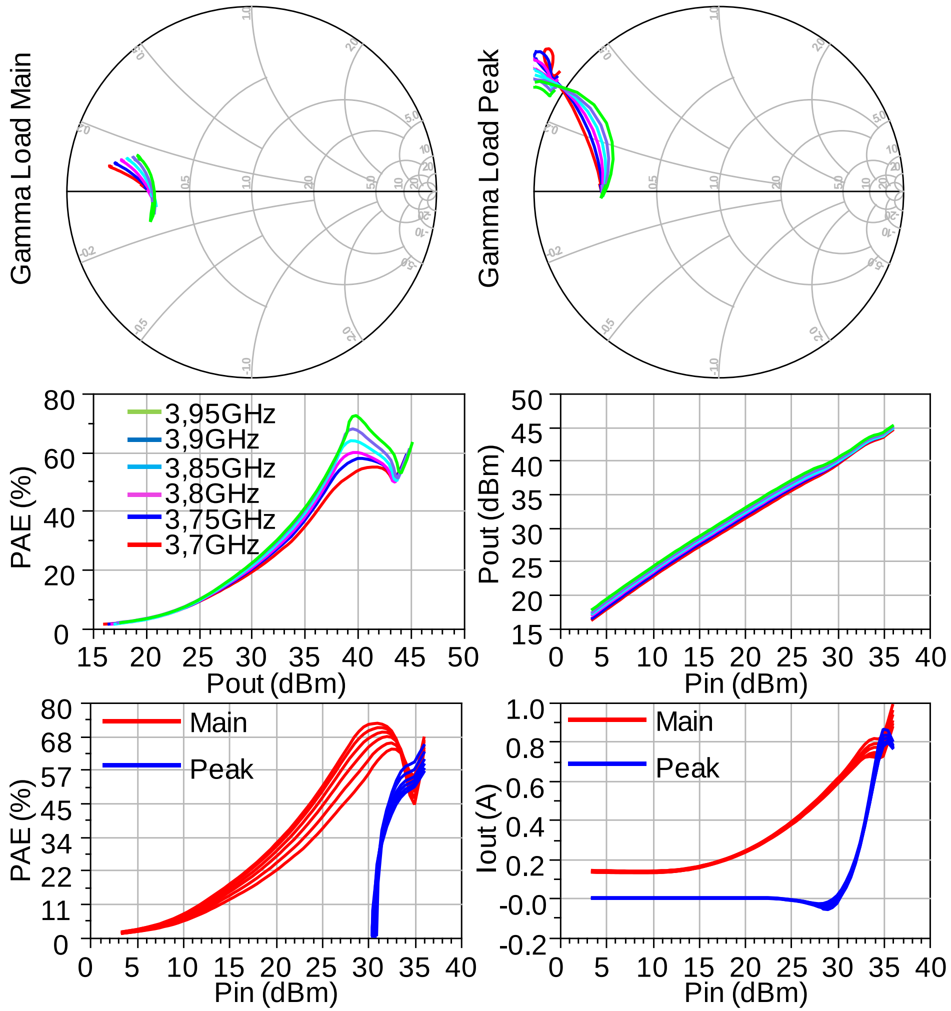
- **EPHD extraction for 3,7 & 3,95 GHz**

EPHD extraction area
including Z_{Opt_PAE} and Z_{Opt_Pout}

Frequency interpolation capabilities

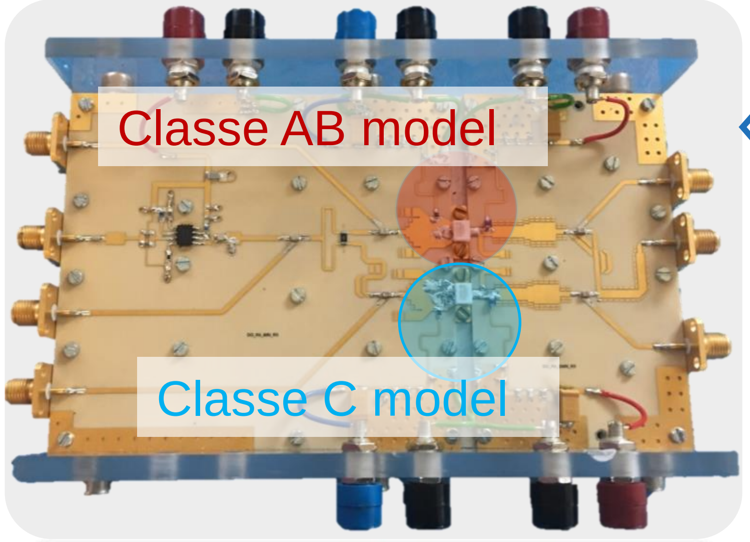
Convergence

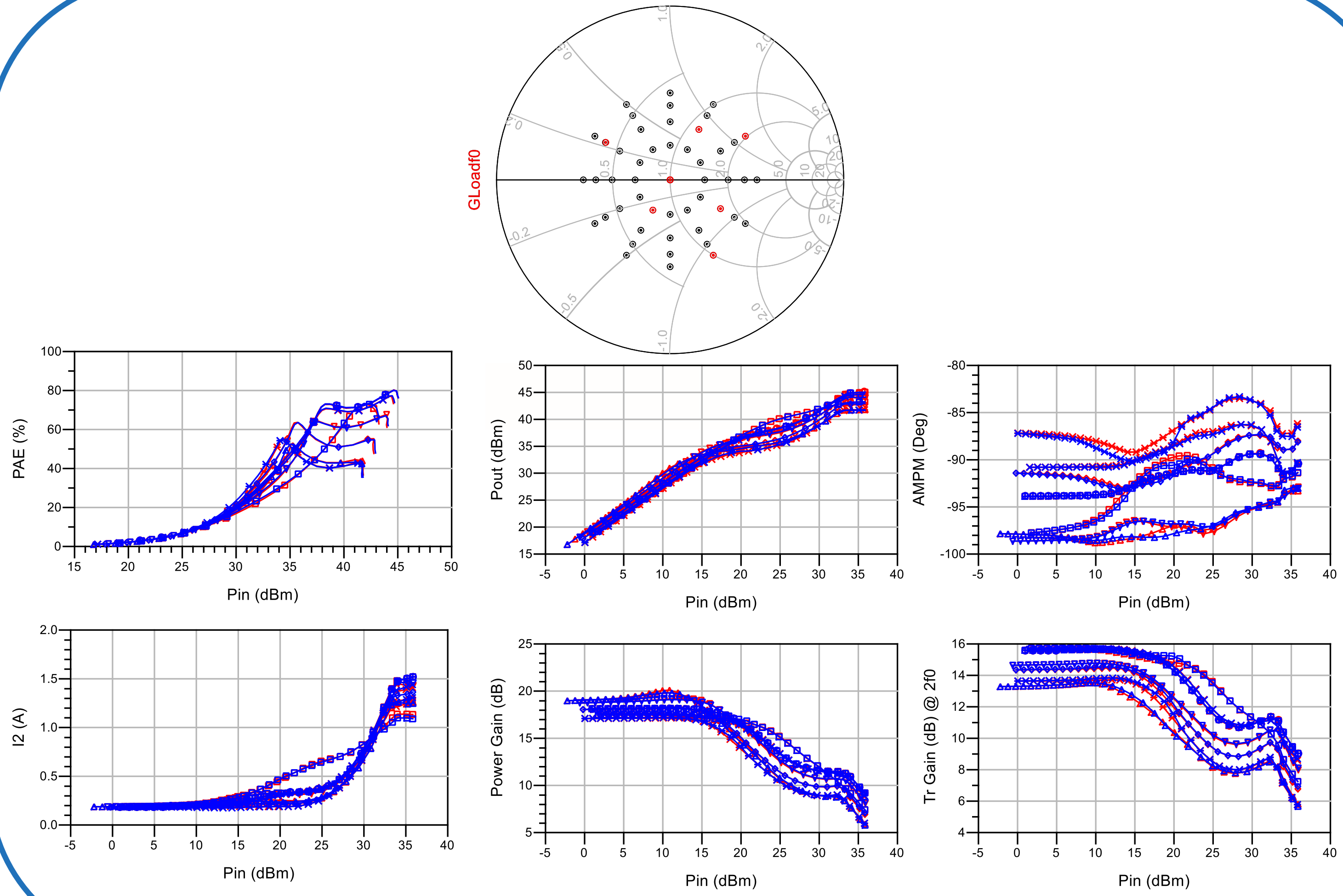
Dynamic variation of the load impedance



EPHD: Circuit Realization

- Doherty PA realization in band [3,7 - 3,95 GHz]





Benchmarking Conclusion

- Strong model robustness for simulations in both AB and C Class (with strong NL behavior regarding the gain curve shape)
- Strong model robustness for dynamic load modulation (extrapolated impedance have been verified)
- Accurate to simulate harmonic behavior
- Ability of the EPHD to predict the overall Design performances without any convergence issues even for extrapolated loading conditions.
- Proof of concept has been made on a real test case
- EPHD model extraction is a software module part of the IVCAD catalogue (already sold as a turnkey solution)
- The EPHD is a promising candidate for the design and realization of power amplifiers of future telecommunication systems due to its robustness and reliability.

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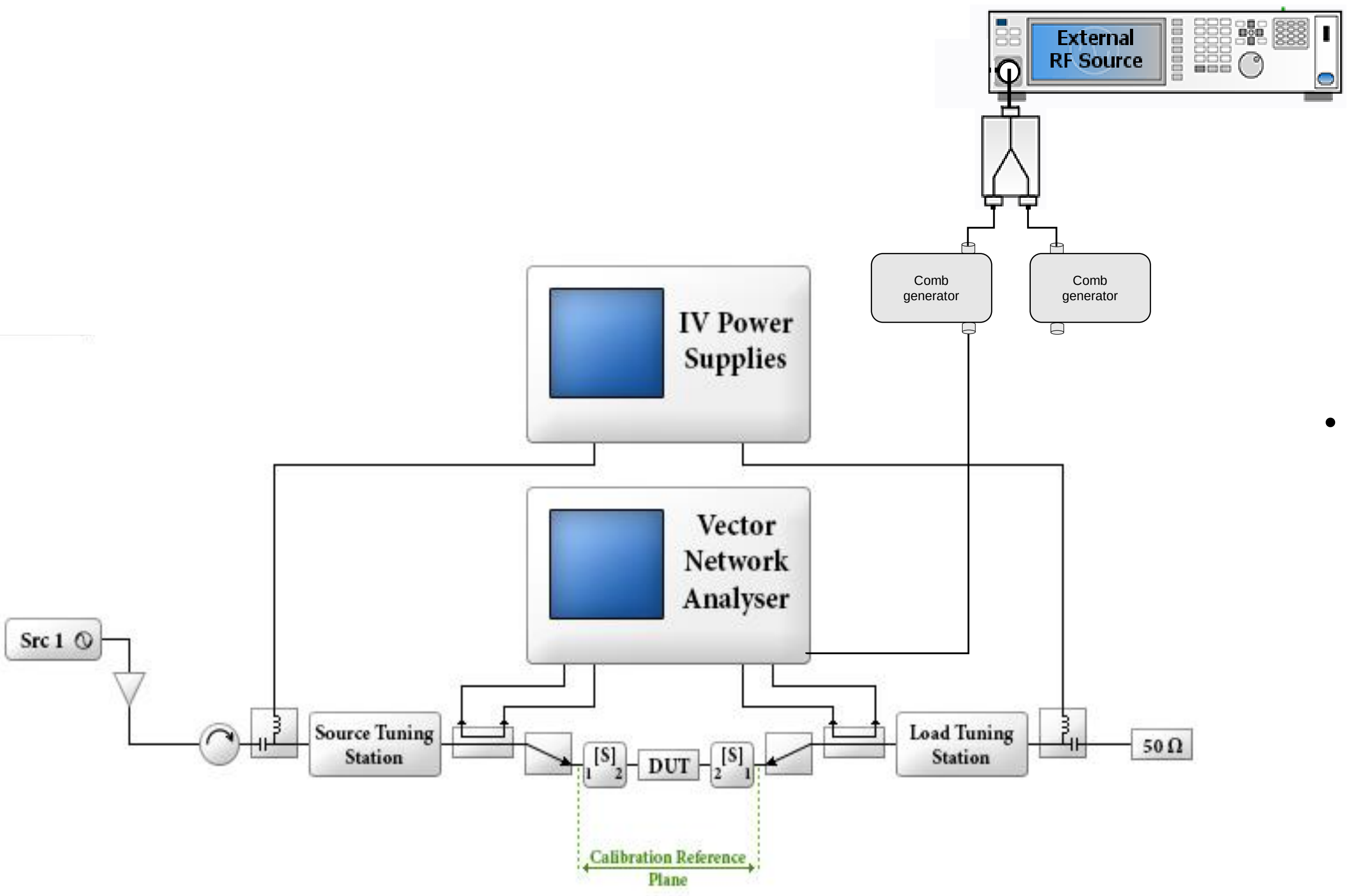
EPHD description

EPHD model packaged transistors

Benchmarking

Measurement Bench & Methodology

Measurement bench

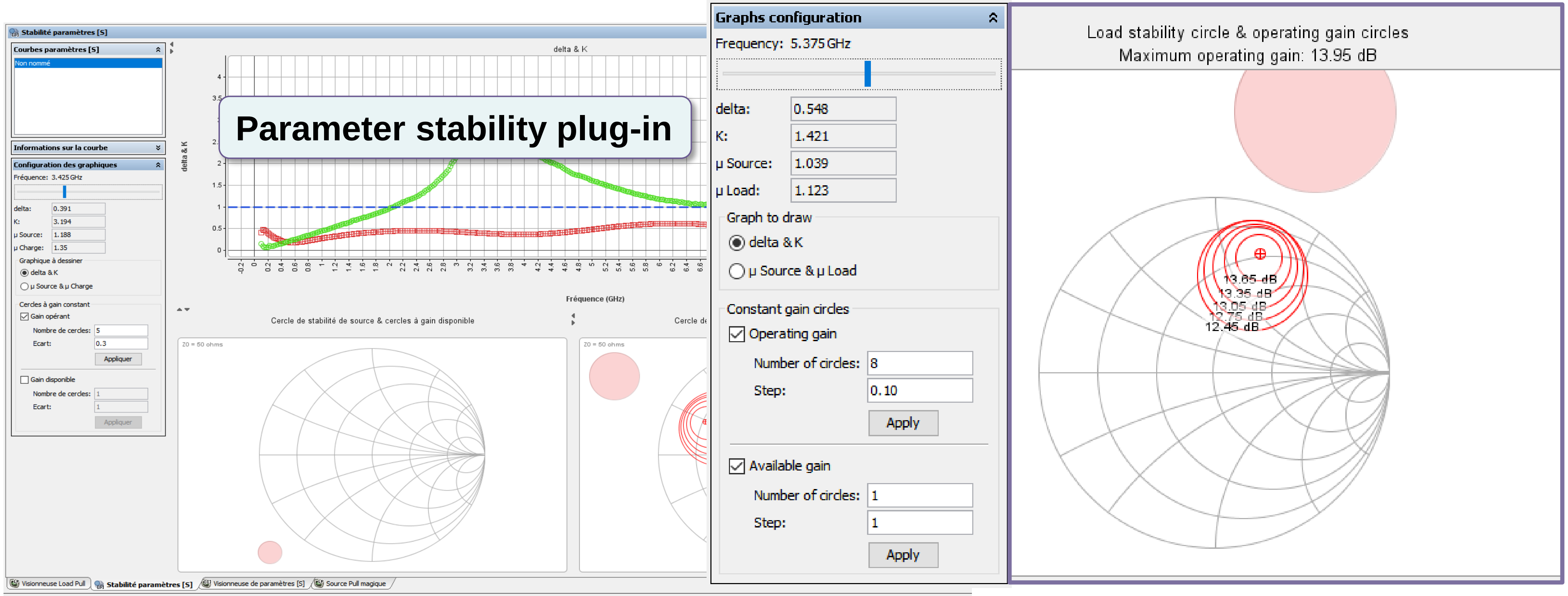


- **Hardware :**
  - Vector Network Analyzer
  - Power Meter
  - Instrumentation driver
  - Circulator
  - Couplers
  - Fundamental & Harmonic tuner (passive, hybrid or active)
  - Comb generator (+ External RF Source)
  - Power Supply (DUT Bias)
- **Software :**
  - **IVCAD**
  - ➢ Vector Receiver Load Pull (MT930C)
  - ➢ Time domain waveform LSA (MT930GA)
  - ➢ EPHD model extraction (MT930R1)
  - ➢ Basic Visualisation (MT930B1)
  - ➢ Advanced Visualization (MT930B2)
  - ➢ Measurement Toolbox (MT930P)
  - ➢ *Active Load Pull (MT930H) optional*

Extraction methodology (1)

1 → First step : location of optimum Gain on linear condition

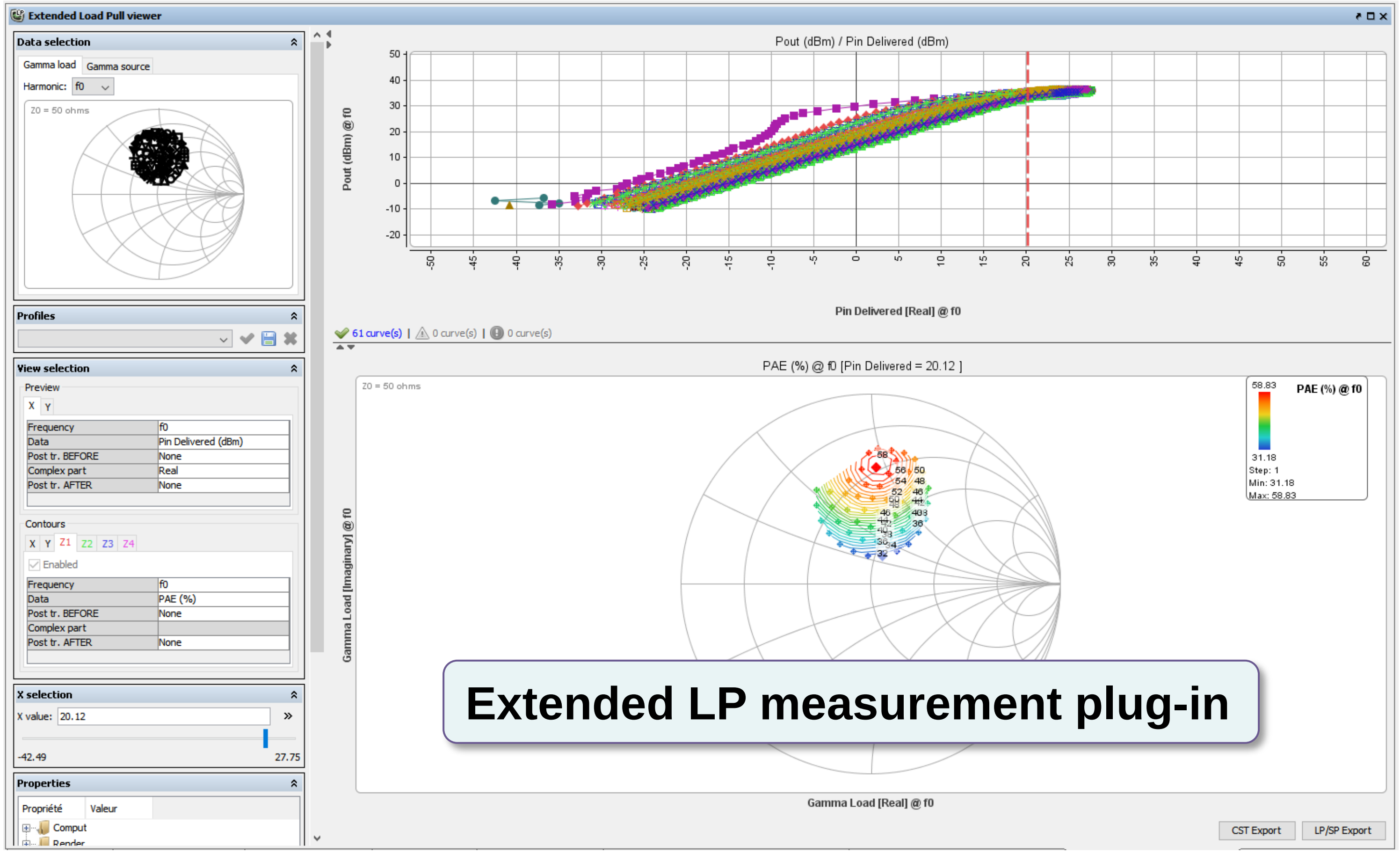
→ S parameter data or measurement – IVCAD ideal matching [S22*]



Extraction Methodology (2)

2 → Second step : Search of PAE/ Pout optimum @ f0

→ PS/IS with pattern f0 definition with High resolution (~60 curves)

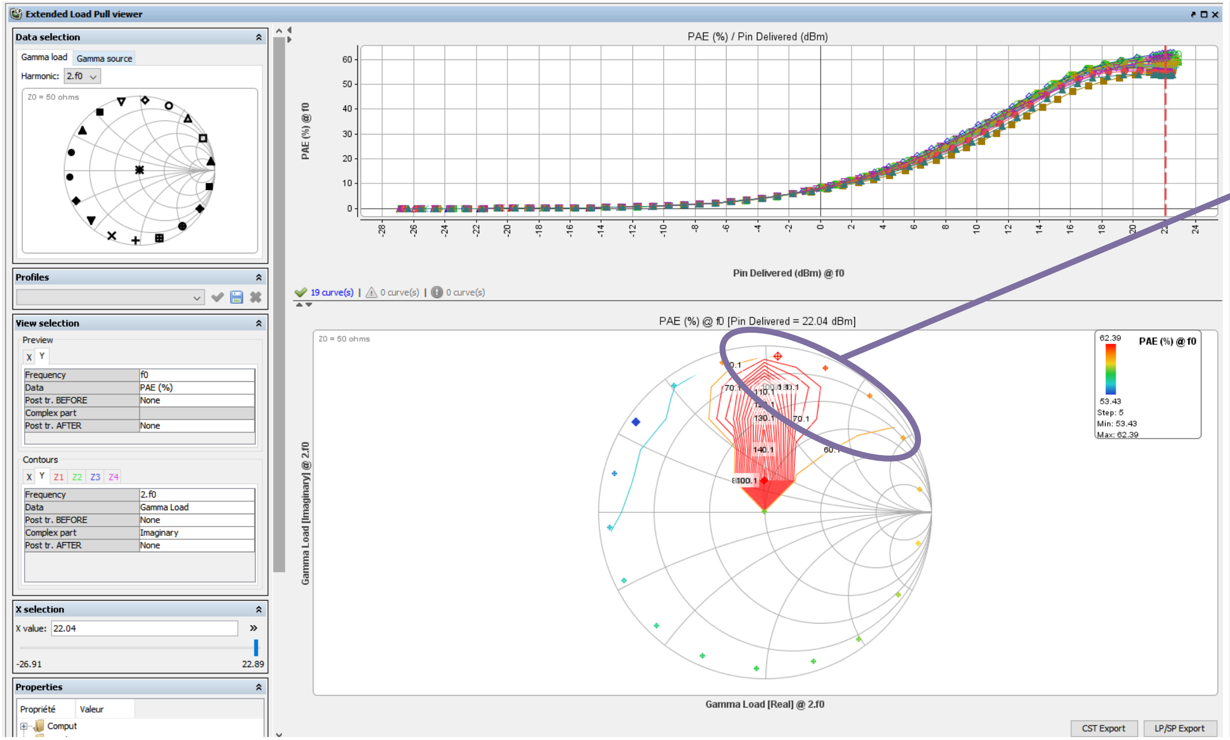


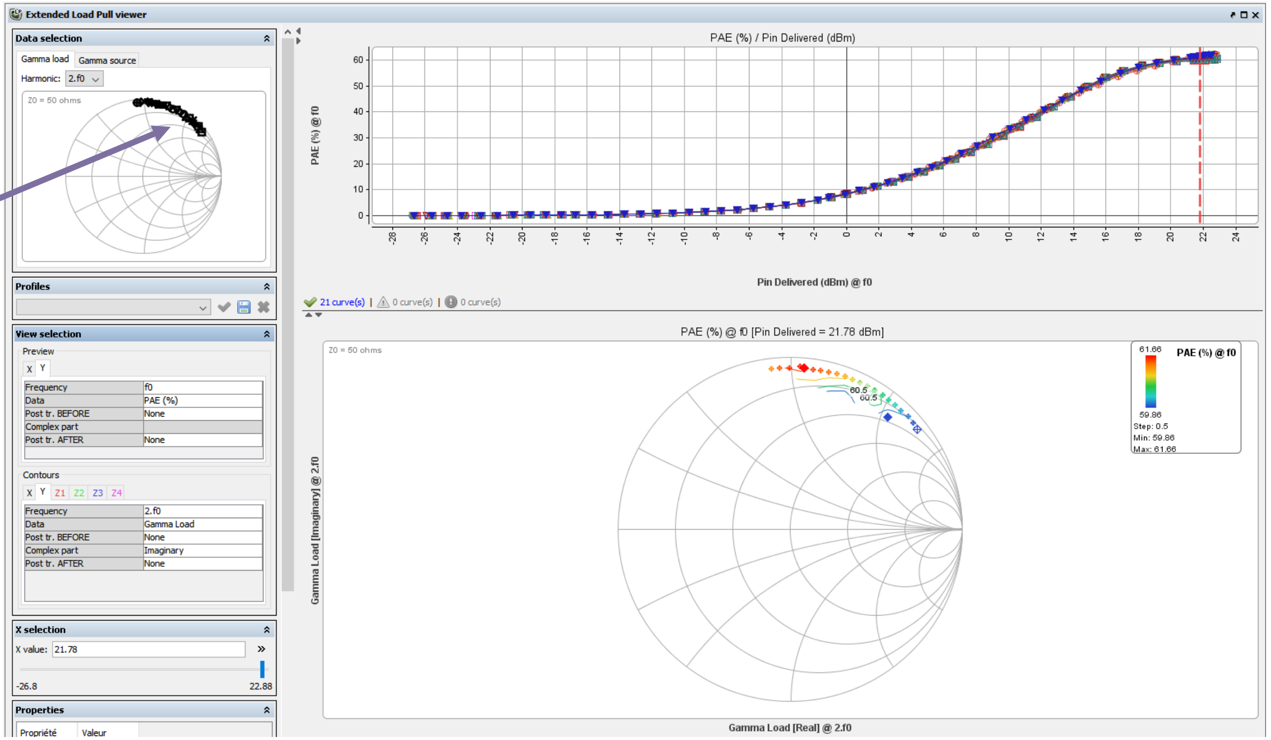
Extended LP measurement plug-in

Extraction Methodology (3)

3 → Third step : harmonic influence (nf0, n>1) [mf0 with m<n on Opt PAE]

→ Example : pattern 2f0 definition with High gamma settings (~20 curves)





Extraction Methodology (4)

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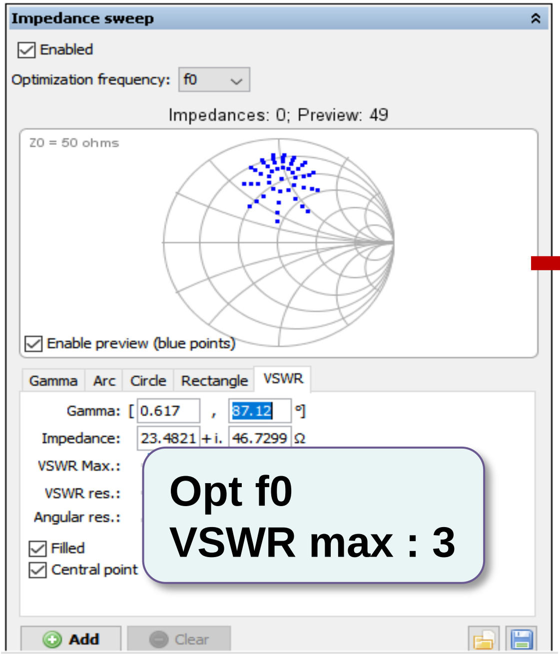
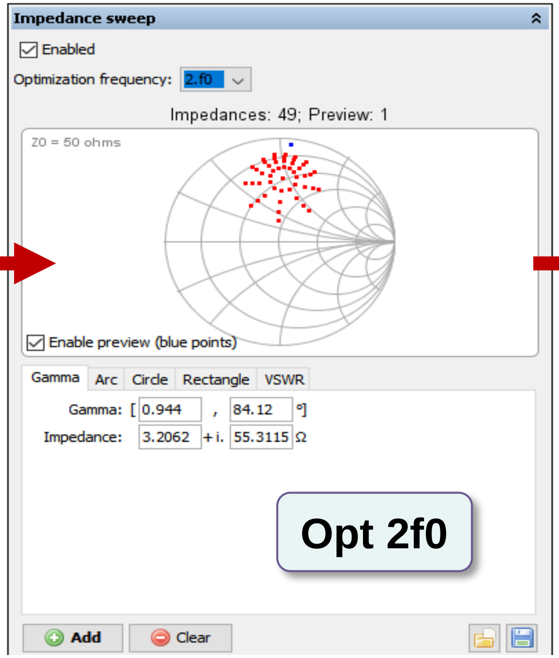
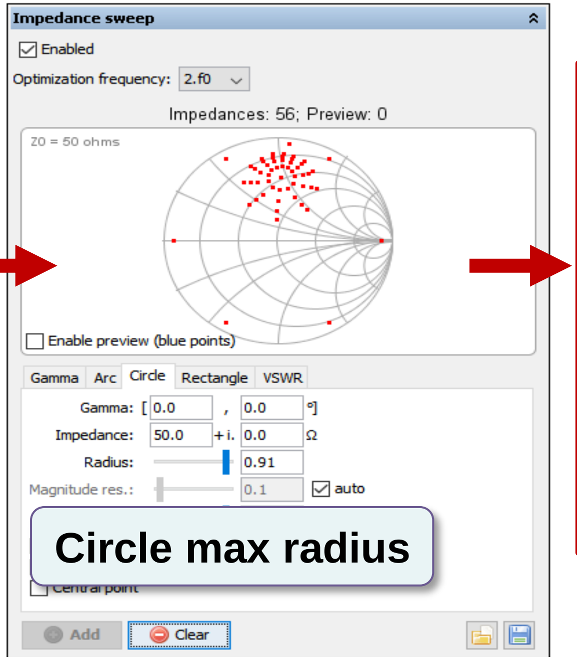
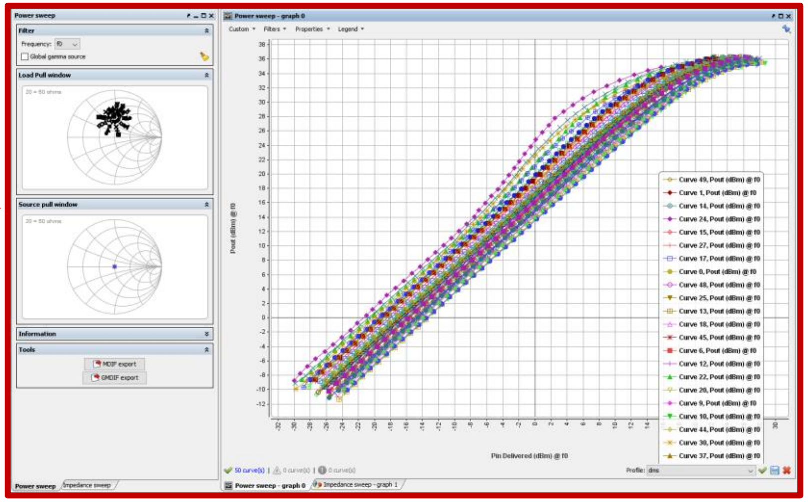
4 Fourth step : pattern definition for EPHD extraction]

Setup & Measurement plug-in – LP Measurement – Power Sweep

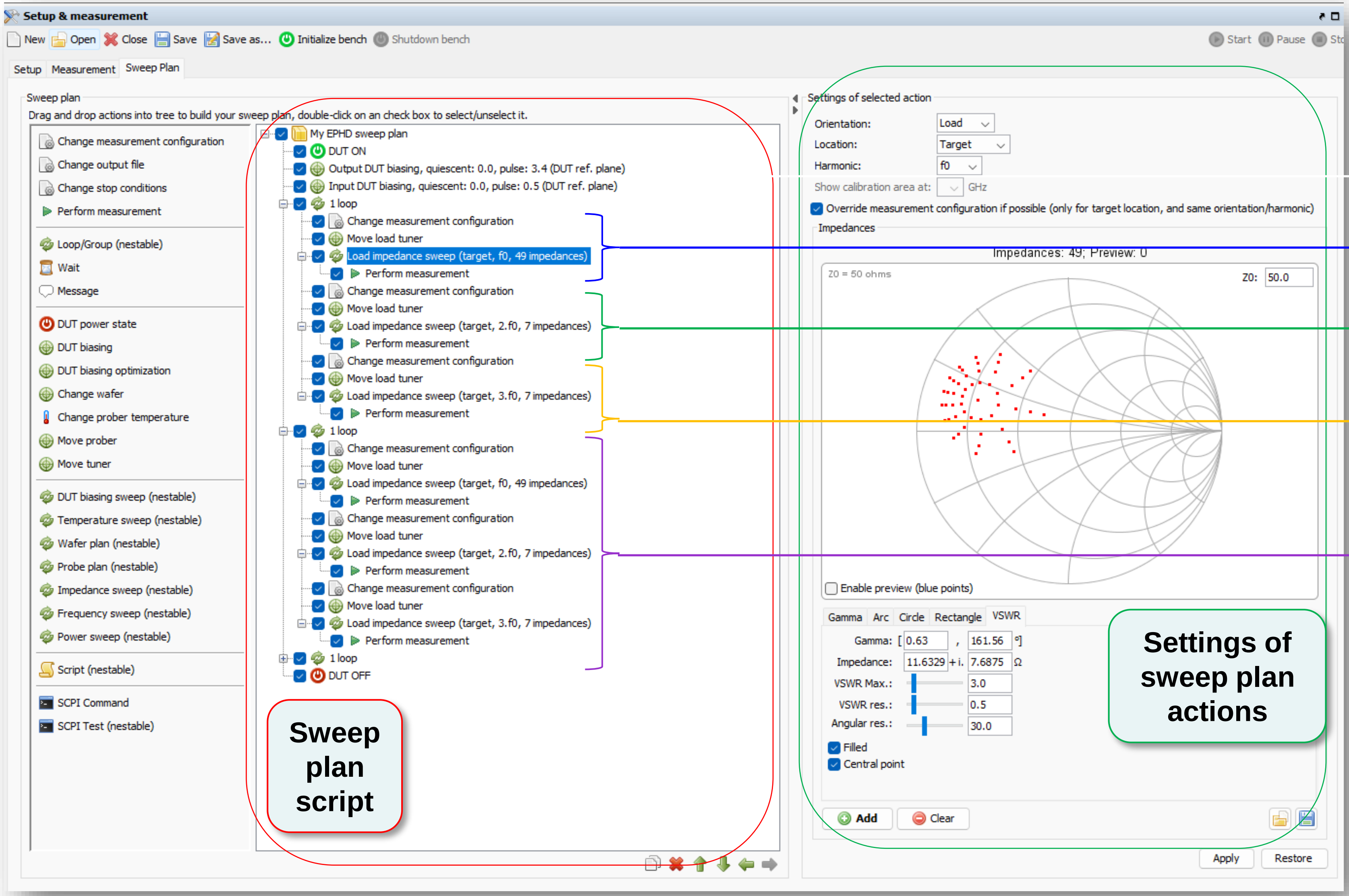








EPHD Using IVCAD : Sweep plan Measurement



DUT bias

Impedance sweep @ f0 (49)

Impedance sweep @ 2f0 (7)

Impedance sweep @ 3f0 (7)

Other loops for other frequencies

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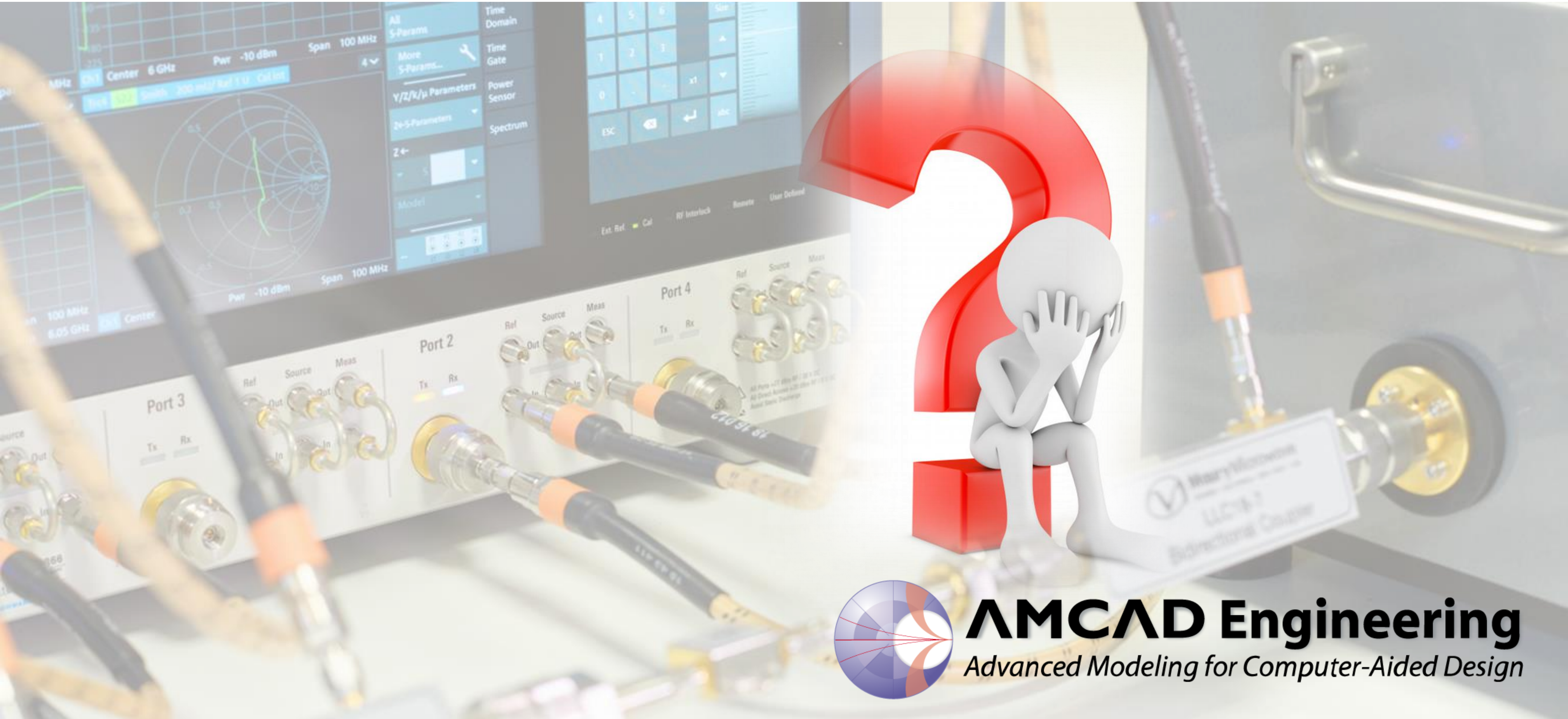

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